

AMENDMENTS TO THE CLAIMS

1. (Previously presented) A circuit comprising:
a surge suppressing circuit comprising first and second transistors which are arranged as a complementary Darlington pair.
2. (Previously presented) A circuit as set forth in claim 1, further comprising:
a resistor connected between the emitter of the first transistor and the base of the second transistor; and
a Zener diode connected between the base of the second transistor and ground.
3. (Previously presented) A circuit as set forth in claim 1, wherein the first transistor is a PNP type transistor and wherein the second transistor is a NPN type transistor
4. (Previously presented) A circuit as set forth in claim 1, wherein the collector of the second transistor is connected to the base of the first transistor.
5. (Currently amended) A circuit as set forth in claim 2, further comprising a diode ~~circuited~~ which is electrically connected with the emitter of the first transistor.
6. (Original) A circuit as set forth in claim 2, wherein the resistor is connected to a junction between the diode and the emitter of the first transistor.
7. (Previously presented) A circuit as set forth in claim 2, further comprising a capacitor connected between ground and the base of the second transistor and in parallel with the Zener diode.
8. (Previously presented) A method of surge suppression comprising interposing a surge suppressing complementary Darlington pair between an input and output.
9. (Original) A method as set forth in claim 8, wherein the complementary Darlington pair is configured by:
using a PNP transistor as the first transistor;

using a NPN transistor as the second transistor; and
connecting the base of the first transistor to the collector of the second transistor

10. (Original) A method as set forth in claim 9, further comprising:
arranging a resistor between the input and a base of the second transistor; and
connecting the base of the second transistor to ground via a Zener diode.